16. (Amended) The method of claim 12, wherein the step of polishing comprises inserting the fluid consisting essentially of water between the semiconductor topography and the abrasive polishing surface.

22. (Amended) A method for processing a semiconductor topography, comprising polishing a dielectric layer with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid consisting essentially of water for reducing a required thickness of an additional layer underlying the dielectric layer.

29. (Amended) The method of claim 22, wherein the step of polishing comprises applying a fluid substantially free of particulate matter between the semiconductor topography and an abrasive polishing surface.

30. (Amended) The method of claim 22, further comprising etching the dielectric layer subsequent to the step of polishing the dielectric layer.

REMARKS

The Specification has been amended to correct typographical errors only and, thus, does not present new matter. In addition, claims 20 and 21 have been canceled and claims 1, 4, 12, 16, 22, 29, and 30 have been amended. Thus, claims 1-19 and 22-30 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Section 112 Rejection

Claims 20 and 21 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. To expedite prosecution, claims 20 and 21 have been canceled rendering rejection thereto moot.

Section 102 Rejections

Claims 12-14, 17, 18, 20 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. 11-177,058 to Atsushi (hereinafter "Atsushi"). In addition, claims 12-14, 17, 18, 20 and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,265,315 to Lee et al. (hereinafter "Lee"). Furthermore, claims 1, 2, 5, 6, 12-14, 19 and 21 were rejected under 35 U.S.C.

§ 102(b) as being anticipated by U.S. Patent No. 6,063,689 to Chen et al. (hereinafter "Chen '689"). Moreover, claims 1, 2, 5, 12-14 and 19-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,136,713 to Chen et al. (hereinafter "Chen '713").

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. The cited art does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art teaches or suggests polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. Amended independent claim 1 states in part: "[a] method for fabricating a shallow trench isolation region, comprising ... polishing said semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter ... ." Amended independent claims 12 and 22 recite similar limitations. Support for the amendments of claims 1, 12, and 22 may be found in the Specification, for example, on page 21, lines 1-15.

Atsushi discloses a semiconductor device and flattening method, which includes a grinding method and etchback method for flattening a layer of insulation film (Atsushi, Detailed Description, paragraph 0024). Atsushi, however, does not teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. Instead, Atsushi specifically teaches the grinding method is a "chemical machinery grinding (Chemical Mechanical Polishing; CMP) method" (Atsushi, Detailed Description, paragraph 0034).

As commonly known in the art, conventional CMP methods are used to planarize or flatten the surface of a semiconductor wafer by selectively removing material from the surface of the wafer through a combination of chemical stripping and mechanical polishing. In some cases, conventional CMP methods may rotate a polishing pad relative to a semiconductor wafer, while depositing an "abrasive, fluid-based chemical suspension, often referred to as a 'slurry'... onto the surface of the polishing pad." (Specification, page 2, lines 20-21). In this manner, the "rotational movement of the polishing pad relative to the wafer causes abrasive particles entrained within the slurry to physically strip the reacted

surface material from the wafer ... to form a planarized surface." (Specification, page 2, lines 23-27, emphasis added).

Therefore, in the absence of teaching a process other than a conventional CMP process, Atsushi implicitly teaches polishing a semiconductor topography with a fluid containing abrasive particulate matter. Thus, Atsushi does not teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter, as recited in present claims 1, 12, and 22. Consequently, Atsushi does not teach or suggest all limitations of present claims 1, 12, and 22.

Lee discloses a method for improving chemical/mechanical polish uniformity over rough topography for semiconductor integrated circuits (Lee, Title). Lee, however, does not teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. Instead, Lee explicitly teaches a CMP method in which "polishing is achieved using a polishing tool and a polishing slurry containing an abrasive such as SiO2." (Lee, column 4, lines 40-41). Consequently, Lee does not teach or suggest all limitations of present claims 1, 12, and 22.

Chen '689 discloses a method for forming an isolation (Chen '689, Title). Chen '689, however, does not teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. Instead, Chen '689 teaches "[a]fter a CMP process is performed on the oxide layer 116 ... micro scratches are formed on the surface of the remains of the oxide layer 116" (Chen '689, column 3, lines 41-44). In addition, Chen '689 explicitly teaches the CMP process includes a slurry containing polishing particles responsible for generating the micro scratches on the surface of the semiconductor topography (*see* Chen '689, column 2, lines 1-2, column 3, line 52 and Fig. 2c). Consequently, Chen '689 does not teach or suggest all limitations of present claims 1, 12 and 22.

Similar to Chen '689, Chen '713 discloses "[a] method for forming a shallow trench isolation (STI) structure [that] adds an etching back process to a conventional method which only uses a chemical mechanical (CMP) process to accomplish the STI structure." (Chen '713, Abstract). Chen '713, however, does not teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. Instead, Chen '713 teaches "grinding particles involved in the CMP process may scratch the STI structure,

resulting in microscratches." (Chen '713, column 3, lines 14-15). As such, Chen '713 explicitly teaches a conventional CMP process, which polishes a semiconductor topography in the presence of a fluid containing abrasive particulate matter (i.e., grinding particles). Consequently, Chen '713 does not teach or suggest all limitations of present claims 1, 12, and 22.

None of the cited art teaches or suggests polishing a semiconductor topography with an abrasive polishing surface in the presence of a fluid consisting essentially of water. Amended independent claim 22 states in part: "[a] method for processing a semiconductor topography, comprising polishing a dielectric layer with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid consisting essentially of water ... ." Amended dependent claims 4 and 16 recite similar limitations. Support for the amendments of claims 4, 12, and 16 may be found in the Specification, for example, on page 21, lines 1-15. In particular, the Specification states, "[t]he fluid applied to the polishing surface in a fixed abrasive process may include deionized water ... [t]he fluid may be used to wash away contaminants resulting from the polishing process." (Specification, page 21, lines 10-13). As such, the Specification explicitly teaches a polishing process, which does not involve the use of a chemical reactant, and thus, is significantly different from a conventional chemical/mechanical polishing (CMP) process.

As stated above, each of the cited art references teaches a conventional CMP process, i.e., a chemical/mechanical polishing process, which includes the use of a slurry. As stated in the Specification, a slurry in a conventional CMP process "fills the space between the polishing pad and the wafer surface such that a chemical in the slurry may react with the surface material ... [and the] rotational movement of the polishing pad ... causes the abrasive particles entrained within the slurry to physically strip the reacted surface material from the wafer." (Specification, page 2, lines 21-25, emphasis added). In this manner, and as stated above, conventional CMP processes typically employ a combination of chemical stripping (i.e., through the use of a chemical reactant within the slurry) and mechanical polishing to form a planarized surface. Therefore, conventional CMP processes do not typically polish a semiconductor topography with an abrasive polishing surface in the presence of a fluid consisting essentially of water, as recited in present claim 22. Since Atsushi, Lee, Chen '689 and Chen '713 each teach a conventional CMP process, Atsushi, Lee, Chen '689 and Chen '713 do not teach all limitations of present claim 22.

For at least the reasons set forth above, the cited art does not teach or suggest all limitations of claims 1, 12, and 22. Therefore, claims 1, 12, and 22 as well as claims dependent therefrom, are asserted to be patentably distinct over the cited art. Accordingly, removal of the § 102 rejections of claims 1, 2, 5, 6, 12-14, 17, 18 and 19 is respectfully requested.

Section 103 Rejections

The Office Action references the obligation of the Applicant under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. §§ 102(e), (f), or (g) prior art under 35 U.S.C. § 103(a). In response, the Applicant asserts that the subject matter of the various claims was commonly owned at the time the application was filed.

Claims 3, 4, 6-11, 15, 16, 22-27, 29, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen '713. In addition, claims 3, 4, 7-11, 15, 16, 20, 22-27, 29, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen '689. Furthermore, claims 15, 16, 22-26, and 28-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee. Moreover, claims 5-16, 22-26, and 28-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Atsushi.

To establish a case of *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A 1974), MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), MPEP 2143.01. The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art can be modified or combined to teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. As stated above, amended independent claims 1, 12, and 22 each disclose a method for polishing a semiconductor topography with an abrasive polishing surface (i.e., a fixed abrasive pad) in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter (i.e., free of abrasive particles).

As noted above in the § 102 arguments, none of the cited art teaches or suggests polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. In fact, the Office Action admittedly states that Atsushi, Lee, Chen '689 and Chen '713 each "fail to disclose ... the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the" respective dielectric layers discussed in the cited art (*see* Office Action, pages 5, 7, 10, and 11). Since none of the cited art teaches or suggests the aforementioned limitation of claims 1, 12, and 22, the cited art cannot be combined to teach or suggest the aforementioned limitation of claims 1, 12, and 22.

Furthermore, the cited art cannot be modified to teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter. The mere fact that references can be ... modified does not render the resultant [modification] obvious unless the prior art also suggests the desirability of the [modification]. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01.

For example, the Specification teaches a modified CMP process, such as a "fixed abrasive polishing process, which is a polishing process in which abrasive material is fixed into the polishing pad rather than being suspended in a liquid to form a slurry." (Specification, page 8, lines 21-24). In addition, the Specification teaches, "contrary to some CMP processes, the polishing rate of the fixed abrasive polishing process is significantly reduced upon forming a substantially planar surface. As such, a fixed abrasive polishing process may be programmed to run longer than a CMP process ... [thereby providing] an over polishing technique ... used to insure that a substantially planar surface has been obtained." (Specification, page 8, lines 25-29). In this manner, the Specification clearly teaches a desirability to modify a conventional CMP process. Such a modification would desirably reduce the polishing rate upon forming a substantially planar surface by polishing a semiconductor topography with an abrasive polishing surface in the presence of a fluid that is substantially free of particulate matter.

In contradiction, none of the cited art suggests a desirability to modify a conventional CMP process to include a fixed abrasive polishing process, as taught in the Specification and the present claims. For example, none of the cited art suggests the desirability to reduce the polishing rate upon forming a substantially planar surface, as taught in the Specification. Therefore, the cited art cannot be modified to teach or suggest polishing a semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter, as recited in present claims 1, 12, and 22. Furthermore, even if the cited references were deemed to teach a fixed abrasive

polishing process (which they do not), the Examiner must also produce evidence that the hypothetical teaching provides motivation to suggest the desirability to be modified to extend a fixed abrasive polishing process to the presently claimed, two-step polish and etchback process.

The Examiner, however, takes official notice that "[i]t would have been obvious to one skilled in the art to employ a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles ... [since such a combination] is a conventional or at least well known means for conducting a cmp polishing process in the semiconductor arts." (*see* Office Action, pages 6, 8, 10 and 11). In response, the Applicant respectfully traverses the above Office Action statement and requests that the Examiner provide a reference in support of his position (*see* MPEP 2144.03). In addition, the Applicant respectfully requests that the Examiner provide a reference in support of the official notice taken with respect to the obviousness of forming an etch mask out of an oxide, a doped oxide such as BPSG, SiC, or a carbonated polymer (see Office Action, pages 6 and 8).

For at least the reasons set forth above, the cited art does not teach or suggest, either separately or in combination, all limitations of claims 1, 12, and 22. Therefore, claims 1, 12, and 22 as well as claims dependent therefrom, are asserted to be patentably distinct over the cited art. Accordingly, removal of the § 103 rejections of claims 3-16 and 22-30 is respectfully requested.

In addition to being patentably distinct for reasons set forth above, several of the dependent claims are believed to be separately patentable for reasons set forth below.

In regard to dependent claim 3, none of the cited art teaches or suggests an upper surface of remaining portions of trench fill material is less than approximately 200 angstroms above the upper surface of the semiconductor substrate. For example, Atsushi specifically teaches polishing the surface part of the layer insulation film 13, such that 100-200 nm (i.e., 1000-2000 angstroms) of layer 13 remains overlying layer insulation film 12 (see Atsushi, Detailed description, paragraph 0034 and Drawing 2(a)). Similarly, Lee specifically teaches "second insulating layer 18 is chemically/mechanically polished (CMP) back to within a few thousand Angstroms (1000-2000 Angstoms) of the etch-stop layer 16 over the electrically conducting layer 12." (Lee, column 4, lines 36-39 and Fig. 2). In addition, neither Chen '689 nor Chen '713 even mention polishing an upper surface to an elevation less than approximately 200 angstroms above the upper surface of the semiconductor substrate, as recited in dependent claim 3. Therefore, claim 3 is asserted to be patentably distinct over the cited art.

Request for Consideration of Information Disclosure Statement

Applicant filed an Information Disclosure Statement accompanied by a Form PTO-1449 on August 8, 2001. To date, Applicant has not received notification that the references cited in the properly filed Information Disclosure Statement have been considered. Applicant hereby requests that the Examiner initial and return the Form PTO-1449 included with the Information Disclosure Statement of August 8, 2001 or indicate in some other way that the references cited therein have been considered.

CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed July 25, 2002. In view of the remarks traversing the rejections presented in the Office Action, Applicants assert that pending claims 1-19 and 22-30 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

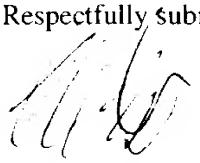
No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-04700.

PETITION UNDER 37 C.F.R. § 1.136 FOR EXTENSION OF TIME

Applicant respectfully petitions the Commissioner for a one-month extension of time under 37 C.F.R. § 1.136 within which to respond to the Office Action mailed July 25, 2002, such extension allowing the undersigned until November 25, 2002 to respond.

The Commissioner is authorized to charge the required fee ($110.00), or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-04700.

Respectfully submitted,



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ATTACHMENT A
"Marked-Up" Amendments

IN THE SPECIFICATION

Please amend pg. 23, line 11 - pg. 24, line 3, as follows:

In an alternative embodiment, the polishing process may be designed to terminate at an elevation within intermediate layer 33. As such, the polishing process may terminate above or within intermediate layer 33, including above or within dielectric 32 and/or layer 34. In this manner, the polishing of underlying layer 42 may be substantially terminated upon exposing layer 34 or dielectric 32. Consequently, structures or layers formed upon semiconductor layer 20 laterally adjacent to intermediate layer 33 may also be polished to approximately the same elevation level as intermediate layer 33. In this manner, intermediate layer 33 may serve as an additional layer upon which the polishing process may terminate above or within. Fig. 9 illustrates a polishing process, which polishes upper layer 42 to an elevation within layer 34. In such an embodiment, layer 34 may include any material with similar polishing characteristics to those of upper layer 42. For example, layer 34 may include a layer of doped silicon. In such an embodiment, layer 34 may be etched at a faster rate than lateral portions of upper layer 42. Fig. 10 illustrates such an etch process, thereby etching layer 34, underlying 32, and laterally adjacent regions of upper layer 42 to form isolation regions 48. As shown in Fig. 10, step height 50 may be formed due to the different etch characteristics of layer 34 and upper layer 42. The thickness of step height 50 may depend on the thickness of layer 34 and 32 in Fig. [14]9. As with step height 46 of Fig. 8, step height 50 is preferably less than approximately 200 angstroms above the top of trenches 40. In one embodiment, the upper surface of the remaining portions of upper layer 42 may be less than approximately 50 angstroms above the top of trenches 40. Alternatively, the upper surface isolation regions 48 may be substantially coplanar with the upper surface of semiconductor layer 20 or below the upper surface of semiconductor layer 20 (not shown).

Please amend pg. 24, lines 5-19, as follows:

Fig. 11 illustrates a polishing process which polishes upper layer 42 subsequent to Fig. 4 to an elevation within layer 32. In such an embodiment, the polishing process may polish through layer 34 or alternatively, layer 34 may have been omitted from the formation of the topography. The entirety of the polished upper surface may then be etched as illustrated in Fig. 12 to form isolation regions 52. In an embodiment in which layer 32 comprises a grown oxide, layer 32 may etch at slightly slower rate than the

deposited dielectric material of upper layer 42. As such, a negative step height may result as shown in Fig. 12. More specifically, the upper surface of upper layer 42 may be below the upper surface of semiconductor layer 20. However, step height [50]54 may be minimal such that laterally adjacent active devices may still be sufficiently isolated. Preferably, the upper surfaces of isolation regions 52 may be less than 200 angstroms below the upper surface of semiconductor layer 20. In one embodiment, the upper surfaces of isolation regions 52 may be less than 50 angstroms below the upper surface of semiconductor layer 20. Alternatively, the upper surfaces of isolation regions 52 may be substantially coplanar with the upper surface of semiconductor layer 20 (not shown).

IN THE CLAIMS

Please cancel claims 20 and 21. Please amend claims 1, 4, 12, 16, 22, 29, and 30 as follows:

1. (Amended) A method for fabricating a shallow trench isolation region, comprising:

blanket depositing a trench fill material over a semiconductor topography comprising one or more trenches;

polishing [said] the semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter to form an upper surface of the semiconductor topography at an elevation above the trenches, wherein the upper surface does not comprise a polish stop material; and

etching an entirety of the upper surface simultaneously, wherein remaining portions of the trench fill material are laterally confined within the trenches.

4. (Amended) The method of claim 1, wherein [said] the step of polishing comprises [a fixed abrasive polishing process] inserting the fluid consisting essentially of water between the semiconductor topography and the abrasive polishing surface.

12. (Amended) A method for processing a semiconductor topography, comprising:

polishing an upper layer of said semiconductor topography with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter to form an upper surface of the semiconductor topography at an elevation above an underlying layer, wherein [said] the underlying layer comprises a lateral variation in polishing characteristics; and

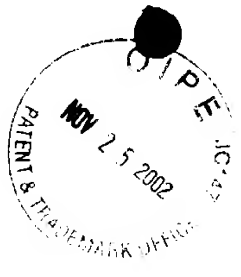
etching the entirety of the upper surface of the semiconductor topography simultaneously to expose the underlying layer.

16. (Amended) The method of claim 12, wherein [said] the step of polishing comprises [a fixed abrasive polishing process] inserting the fluid consisting essentially of water between the semiconductor topography and the abrasive polishing surface.

22. (Amended) A method for processing a semiconductor topography, comprising [using fixed abrasive] polishing [of] a dielectric layer with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid consisting essentially of water for reducing a required thickness of an additional layer underlying the dielectric layer.

29. (Amended) The method of claim 22, wherein [said fixed abrasive] the step of polishing [process] comprises applying a fluid substantially free of particulate matter between the semiconductor topography and an abrasive polishing surface.

30. (Amended) The method of claim 22, further comprising etching the dielectric layer subsequent to [said fixed abrasive] the step of polishing the dielectric layer.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Inventor(s): Gilboa et al.
Serial No.: 09/846,119
Filing Date: 4/30/01
Title: METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE
Atty. Docket No. 5298-04700; PM00028

The date stamp of the mail room of the U.S. Patent and Trademark Office hereon will acknowledge receipt of the attached 1) Response to Office Action mailed July 25, 2002; 2) Information Disclosure Statement w/accompanying Form PTO-1449 and reference B1; and 3) Return Postcard.

KLD\pwg Via First Class Mail date: November 19, 2002